(19) Europäisches Patentamt
European Patent Office
Office uropéen des brevets

(11) Publication number : **0 599 529 A2**

J1040 U.S. PTO
10/029446
12/20/01

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93309121.7**

(51) Int. Cl.[5] : **H04N 7/13**, H04N 7/137

(22) Date of filing : **15.11.93**

(30) Priority : **25.11.92 JP 314815/92**

(43) Date of publication of application :
01.06.94 Bulletin 94/22

(84) Designated Contracting States :
DE FR GB IT NL

(71) Applicant : **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD**
1006, Oaza Kadoma,
Kadoma-shi
Osaka 571 (JP)

(72) Inventor : **Takahashi, Toshiya**
1-5-107, Akeno-cho
Takatsuki-shi, Osaka, 569 (JP)

(74) Representative : **Crawford, Andrew Birkby et al**
A.A. THORNTON & CO.
Northumberland House
303-306 High Holborn
London WC1V 7LE (GB)

(54) Method and apparatus for picture coding and method and apparatus for picture decoding.

(57) Method and apparatus for picture coding and method and apparatus for picture decoding are disclosed, wherein an apparatus for picture coding comprises :

means for receiving and storing picture data composed in frames,

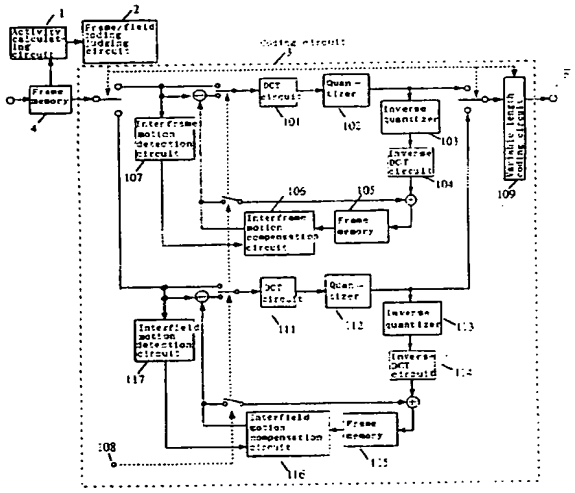
activity calculating means for calculating the activity of the picture data in every frame,

frame/field coding judging means for receiving the activity, and Judging to perform frame unit coding when the activity is over a specific value or to perform field unit coding by dividing a frame into fields when the activity is below a specific value, and

coding means for coding in frame unit or coding in field unit concerning the picture data on the basis of the judgement, and issuing a coded picture signal containing the frame/field coding Judgement signal,

whereby picture coding of high efficiency is realized despite magnitude of motion, by coding in field unit when the motion of picture is large, and coding in frame unit by making use of the vertical correlation of picture when the motion is small.

Fig. 1



EP 0 599 529 A2

The invention relates to method and apparatus for picture coding and method and apparatus for picture decoding, and more particularly to method and apparatus for picture coding and method and apparatus for picture decoding of high efficiency effective for transmission or recording of digital images.

The transfer rate of digital image reaches hundreds of Mbps to several Gbps, and processing of digital image is restricted by the communication cost at the time of transmission, and limited by the recording capacity of the recording apparatus at the time of recording. It has been accordingly attempted to develop method and apparatus for picture coding capable of minimizing the deterioration of picture quality and lowering the transfer rate at the same time.

As one of such picture coding methods, the motion compensation interframe differential two-dimensional discrete cosine transform (DCT) of the CCIR H.261 standard is described below.

Fig. 8 is a block diagram of motion compensation interframe differential two-dimensional DCT. In Fig. 8, numeral 101 denotes a DCT circuit, 102 is a quantizer, 103 is an inverse quantizer, 104 is an inverse DCT circuit, 105 is a frame memory, 106 is an interframe motion compensation circuit, 107 is an interframe motion detection circuit, 108 is an intraframe/interframe changeover circuit, and 109 is a variable length coding circuit.

In this conventional picture coding apparatus, the operation is as follows.

The input is an interlaced image called common intermediate format (CIF). Fig. 9 is a time-space configuration of pixels of input picture, in which the axis of abscissas denotes the time direction and the axis of ordinates represents the vertical direction or the line direction. In the diagram, a set of pixels equal in the time axis is called a CIF frame, and coding is performed in the unit of CIF frame.

The first frame of coding, that is, the picture of frame t is changed over to intraframe coding by an intraframe/interframe changeover signal 108, and is subjected to intraframe coding without considering the difference. That is, the image data is converted into a transform coefficient in the DCT circuit 101 in the unit of two-dimensional block, and the transform coefficient is quantized in the quantizer 102, and is subjected to variable length coding in the variable length coding circuit 109, and is sent out into a transmission route. Generally, the picture is high in correlation, and, as a result of DCT, the energy is concentrated in the transform coefficient corresponding to the low frequency components. Therefore, by quantizing coarsely the high frequency components which are less obvious visually, and finely the low frequency components which are important components, the picture quality deterioration is kept to a minimum, and the quantity of data can be decreased at the same time. The transform coefficient after quantizing is simultaneously returned to the real time data via the inverse quantizer 103 and inverse DCT circuit 104, and accumulated in the frame memory 105.

On the other hand, the pictures after frame (t+1) are subjected to interframe differential coding in each frame. First, in the motion detection circuit 107, by employing, for example, the well-known full search method, the interframe motion vector is determined in every two-dimensional block. The interframe motion compensation circuit 106 generates, making use of the detected motion vector, a predicted value compensating the motion of the next frame in the unit of two-dimensional block. The picture of frame (t+1) is compared with the predicted value generated from frame t in the above method, and the difference or prediction error is calculated. Afterwards, the prediction error is coded in the same manner as in frame t. After frame (t+2), the prediction error is coded in the same manner as in the method of frame (t+1). According to this method, since the prediction error is coded, as compared with the case of directly coding the image data as in the intraframe coding, the energy decreases, and more efficient coding is enabled (for example, refer to CCITT Recommendation H.261, "Codec for audiovisual services at px 64 kbit/s," Geneva, 1990).

In this picture coding method, however, the picture input by interlaced scanning cannot be coded efficiently. The reason is explained by reference to Figs. 10, 11, and 12. The pictures generally used at the present are scanned by interlacing. Fig. 10 is a time-space configuration of pixels of interlaced picture. Figs. 11 and 12 explain examples of display of interlaced picture in frame, without motion in Fig. 11, and with a horizontal motion in Fig. 12.

Pixels are disposed at positions deviated in time in every one vertical line by interlacing. In Fig. 10, a set of pixels equal in the time axis is called a field, and two fields differing in the time axis are put together to form a frame, and one frame is composed of field 1 and field 2. Without motion, as shown in Fig. 11, the frame picture is an image of high vertical correlation. With motion involved, the frame picture is deviated by the amount of interfield motion in every field, that is, in every line as shown in Fig. 12. Therefore, it is efficient to code in the unit of frame in the absence of motion, but in the presence of motion, if coded in the frame unit, a high frequency component in the vertical direction corresponding to the field difference occurs, which causes deterioration of picture quality, and it is hence preferred to employ the conventional image coding method in the field unit. The problem was that the optimum coding method varied depending on the motion, that is, coding in the frame unit in the case of small motion and coding in the field unit in the case of large motion.

It is hence a primary object of th invention to present method and apparatus for picture coding and meth-

od and apparatus for its decoding of high efficiency capable of executing optimum coding despite magnitude of motion of picture.

To achieve the object, one of the preferred embodiments of the invention comprises:

means for receiving and storing picture data composed in frames,

activity calculating means for calculating the activity of the picture data in every frame,

frame/field coding judging means for receiving the activity, and judging to perform frame unit coding when the activity is over a specific value or to perform field unit coding by dividing a frame into fields when the activity is below a specific value, and

coding means for coding in frame unit or coding in field unit concerning the picture data on the basis of the judgement, and issuing a coded picture signal containing the frame/field coding judgement signal,

whereby picture coding of high efficiency is realized despite magnitude of motion, by coding in field unit when the motion of picture is large, and coding in frame unit by making use of the vertical correlation of picture when the motion is small.

Further objects and effects of the invention will be better understood and appreciated in the following detailed description.

Fig. 1 is a block diagram of a first embodiment of a picture coding apparatus according to the invention.

Fig. 2 is an explanatory diagram of coding in frame unit and coding in field unit of the invention.

Fig. 3 is a block diagram of activity calculating circuit 1 and frame/field coding judging circuit 2 in Fig. 1.

Fig. 4 is a flow chart showing processing in frame/field coding judging circuit of the invention.

Fig. 5 is a flow chart showing processing in frame/field coding judging circuit in a second embodiment of the invention.

Fig. 6 is a block diagram of a third embodiment of picture coding apparatus according to the invention.

Fig. 7 is a block diagram of an embodiment of a picture decoding apparatus according to the invention.

Fig. 8 is a block diagram of a conventional motion compensation interframe differential two-dimensional DCT.

Fig. 9 is a time-space configuration diagram of pixels of CIF.

Fig. 10 is a time-space configuration diagram of pixels of interlaced picture.

Fig. 11 is an explanatory diagram of frame picture without motion.

Fig. 12 is an explanatory diagram of frame picture with motion.

Referring now to drawings, a first embodiment of method and apparatus for picture coding according to the invention is described below.

Fig. 1 is a block diagram of a picture coding apparatus according to the first embodiment of the invention, Fig. 2 is an explanatory diagram of coding in frame unit and coding in field unit, Fig. 3 is a block diagram of activity calculating circuit and frame/field coding judging circuit in Fig. 1, and Fig. 4 is a flow chart showing processing in frame/field coding judging circuit 2. In Fig. 1, numeral 1 denotes an activity calculating circuit, 2 is a frame/field coding judging circuit, 3 is a coding circuit, 4 is a frame memory, and 5 is a coded picture output terminal.

The image coding apparatus in Fig. 1 is explained by reference to Figs. 1, 2, 3 and 4.

The input picture in frame unit is stored in the frame memory 4, and at the same time the frame block activity Ar and field block activity Ai are calculated in the activity calculating circuit 1. This activity is calculated, for example, as follows. The input picture is divided into two-dimensional small blocks, and sequentially numbered in the frame unit as shown in Fig. 2 (a), as frame small block Sbr (x,y) (x: horizontal pixel address, $1 \leqq x \leqq 8$, y: vertical pixel address, $1 \leqq y \leqq 8$), and sequentially numbered in the frame unit as shown in Fig. 2 (b), as picture data of field small block Sbi (x,y,n) (x: horizontal pixel address, $1 \leqq x \leqq 8$, y: vertical pixel address, $1 \leqq y \leqq 4$, n: small block address $1 \leqq n \leqq 2$). Consequently, adding the energy sum of interline difference of every line in each block, the frame and field block activities are obtained. They are expressed in the following equations.

[Formula 1]

$$Ar = \sum_{x=1}^{8} \sum_{y=1}^{8,2} (Sbr(x, y+1) - Sbr(x, y))^2$$

$$Ai = \sum_{n=1}^{2} \sum_{x=1}^{8} \sum_{y=1}^{4,2} (Sbi(x, y+1, n) - Sbi(x, y, n))^2$$

Fig. 3 is an example of activity calculating circuit 1, which comprises a buffer memory 11 for dividing the input picture into two-dimensional small blocks, an address generating circuit 12 for generating its address, first and second square error calculating circuits 13, 14 for calculating square errors or Ar, Ai, and a multiplexer 15 for multiplexing and issuing Ar, Ai.

Thus obtained block activities are fed into the frame/field coding judging circuit 2. In Fig. 3, the frame/field coding judging circuit 2 is composed of central processing unit (CPU). Reference is made to Fig. 4 which shows the operation of the CPU. The input frame activity Ar and field activity Ai are compared in magnitude in every two-dimensional block, and the number α of blocks of Ai>Ar in one frame is calculated. Next, α is compared with an experimentally determined value T1, and if $\alpha \geqq T1$, a change-over signal showing frame coding is issued, and if $\alpha < T1$, a changeover signal showing field coding is issued, in every frame.

In the case of small motion, since the correlation of vertical pixels is high, the relation is Ai>Ar. In the case of large motion, to the contrary, the difference between different fields is large, and it is Ai<Ar. Therefore, when T1 is set as 1/2 of the number of blocks in one frame, for example, by comparing Ar and Ai in every block, when the number of blocks α of Ai>Ar occupies the majority in one frame, that frame is judged to be efficient in coding in frame unit. To the contrary, if the number of blocks satisfying Ar>Ai is many, coding in field unit is judged to be appropriate. Herein, coding in frame unit and field unit is coding or decoding in the unit of frame in terms of the time, or in the unit of field, as shown in Fig. 2 (a), (b), respectively. In the frame unit, field 1 and field 2 of time t must be coded and decoded simultaneously, but in the field unit, on the other hand, field 1 and field 2 of time t are coded and decoded at separate times.

The coding circuit 3 employs, for example, a motion compensation interframe differential two-dimensional DCT circuit in the prior art, and a motion compensation interfield differential two-dimensional DCT circuit applying the prior art in the field unit. The main difference between the motion compensation interframe differential two-dimensional DCT circuit and the motion compensation interfield differential two-dimensional DCT circuit are whether the object of coding is the block in frame unit as shown in Fig. 2 (a) or the block in field unit as shown in Fig. 2 (b), and whether the motion detection and motion compensation are frame interval or field interval. Therefore, the difference in circuit lies only in the motion detection circuits 107, 117, and motion compensation circuits 106, 116.

If the result of judgement by the frame/field coding judging circuit 2 is coding in frame unit, the frame memory 4 issues a frame block. In the coding circuit 3, changing over the switch, the frame unit block is fed into the motion compensation interframe differential two-dimensional DCT circuit, and at the same time, the input of the variable length coding circuit 109 is changed over to the quantizer 102 in the motion compensation interframe differential two-dimensional DCT circuit. In the case of coding in field unit, in the same operation as in the frame unit, the block in the field unit is coded.

The result of judgement by the frame/field coding judging circuit 2 is sent out from the output terminal 5, together with the coded picture signal, through the variable length coding circuit 109.

In this picture coding apparatus, when the interframe correlation is higher than the interfield correlation, it follows that $\alpha \geqq T1$, and interframe coding is selected, and in the reverse case, the interfield coding is selected, thereby realizing optimum coding adaptively to the magnitude of the motion.

Fig. 5 is a flow chart showing processing in the CPU of the frame/field coding judging circuit 2 in a second embodiment of the inv ntion. What differs from the first embodiment is that the frame coding and field coding are not changed over in every frame, but only once in every N frames. When the number of blocks α of Ai>Ar satisfies the condition of $\alpha \geqq T1$, the pointer β showing how many frames have satisfied $\alpha \geqq T1$ is added. At the end of N frames, the pointer β is compared with an experimentally determined value T2 (for example T2 = N/2), and if $\beta \geqq T2$, a changeover signal showing frame coding is issued, and if $\beta < T2$, a changeover signal showing field coding is issued.

Usually, in interframe differential coding, in order to prevent error propagation, intraframe coding is inserted in a specific period. In the second embodiment, the period of intraframe coding is regarded as N frames, and the coding in frame unit and coding in field unit are changed over in the intraframe coding period N. Accordingly, changeover of coding occurs only in N frame periods, and the load of the hardware can be alleviated. Besides, if coding in frame unit and in field unit is frequency changed over in every frame, the picture quality may fluctuate, but it is changed over in every N frames in the second embodiment, so that fluctuation of picture quality may be avoided.

In the second embodiment, it is judged by the number of times β occurring in N frames, but in order to further avoid fluctuations of picture quality, it may be also possible to set to change over if occurring x times continuously. In usual pictures, it is very rare that a moving part and a slow moving part are changed over in every frame, but a picture continues for several frames or several seconds. Therefore, by setting N = 15, x = 8, that is, by changing over coding in frame unit or coding in field unit when the majority conforms to the condition continuously during 0.5 sec, a sufficient performance is obtained.

In the foregoing embodiments, the block activities Ar, Ai are determined by the difference between the lines, but it is not limitative, and for example, it may be the sum of the AC energy of frame and field blocks. That is, using Sbr, Sbi in the first embodiment, first the mean values of each small block mr, mi(n) are determined. Then, using mean values mr, mi(n), the AC energy of each small block is determined, and the sum of AC energies of small blocks is calculated to obtain Ar, Ai. They are expressed in the following equations.

[Formula 2]

$$mr = \frac{1}{64} \sum_{x=1}^{8} \sum_{y=1}^{8} Sbr(x, y)$$

$$Ar = \sum_{x=1}^{8} \sum_{y=1}^{8} (Sbr(x, y) - mr)^2$$

$$mi(n) = \frac{1}{32} \sum_{x=1}^{8} \sum_{y=1}^{4} Sbi(x, y, n)$$

$$Ai = \sum_{n=1}^{2} \sum_{x=1}^{8} \sum_{y=1}^{4} (Sbi(x, y, n) - mi(n))^2$$

Judgement of coding in frame unit and coding in field unit is done on the basis of the total number of blocks conforming to the conditions by comparing Ai and Ar in each block, but it is not limitative, and the entire picture may be regarded as one block, and comparison of Ai>Ar is determined only once in every frame, and it is judged on the basis of the result, so that same effects may be obtained.

In comparison of block activities Ai, Ar, it is judged at Ai>Ar in the foregoing embodiments, but by adding an offset it is also possible to judge at (Ai + offset) > Ar. Generally, frame unit coding is more efficient than field unit coding, and hence by judging with offset, it is possible to increase the frequency of frame unit coding.

In the first and second embodiments, the initial value of coding may be either frame unit coding or field unit coding, but in general picture, small movements are in majority, and it may be set at frame unit coding.

Fig. 6 is a block diagram of a third embodiment of a picture coding apparatus of the invention. What differs from the second embodiment is the constitution of the coding circuit. (In Fig. 6, the coding circuit is indicated by numeral 30.) In the second embodiment, the motion compensation interframe differential two-dimensional DCT circuit and motion compensation interfield differential two-dimensional DCT circuit are changed over by the output of the coding judging circuit 2, but in the third embodiment, the output of the coding judging circuit 2 is fed into an interframe/interfield prediction circuit 126, and it is designed so as to be capable of changing over the motion compensation not only in the block unit but also in the entire picture, so that the coding circuit may be composed of the smaller hardware than in the second embodiment.

Fig. 7 is a block diagram of an embodiment of picture decoding apparatus of the invention. The apparatus in Fig. 7 comprises a frame/field decoding changeover circuit 6, a decoding circuit 7, a coding image input terminal 8, and a picture output terminal 9, and operates as follows. The coded picture input is fed into a variable

length decoding circuit 139 inside the decoding circuit 7, and is separated into the picture data and frame/field coding judging signal. The frame/field decoding changeover circuit 6 receives the frame/field coding judging signal determined by the activity from the variable length decoding circuit 139, and sends the frame/field decoding changeover signal to the decoding circuit 7. The decoding circuit 7 processes the picture data by inverse quantizing and inverse DCT, and compensates the motion in frame unit or field unit depending on the changeover signal in each circuit, reproduces the picture, and issues the decoded picture in frame unit or field unit selected by the changeover signal. Therefore, by the picture decoding apparatus shown in Fig. 7, the picture having being coded by the foregoing embodiments can be decoded.

In the embodiment in Fig. 7, the motion compensation prediction circuit is composed of different circuits in every frame or field, but it is also possible to simplify by using the motion compensation interframe/interfield prediction circuit as shown in Fig. 6.

In these embodiments, as the example of coding circuit, the motion compensation interframe differential DCT circuit is explained, but it is not limitative, and Hadamard transform, Fourier transform, other orthogonal transform circuits, vector quantizing circuits, and any other means having the function of coding the image can be similarly employed.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

Claims

1. A method for picture coding comprising:
   a step of feeding picture data composed of one frame,
   a step of calculating the activity of the picture data in every frame,
   a step of comparing the activity with a specific value, and judging to perform frame unit coding when larger than a specific value, and to perform field unit coding by dividing a frame into fields when the activity is below a specific value.

2. A method for picture coding of claim 1, wherein the step for calculating the activity is to divide the input picture data into one or more two-dimensional blocks, compare the field block activity calculated in field unit and the frame block activity calculated in frame unit, and issue the number of blocks with the field block activity larger than the frame block activity as calculation output of the activities.

3. A method for picture coding of claim 1, wherein the step of changing over between frame unit coding and field unit coding is to change over when the activity is more than or below a specific value continuously in plural frames.

4. A method for picture coding of claim 1, wherein the step of changing over between frame unit coding and field unit coding is to change over with at least one of the predetermined plural changeover points.

5. An apparatus for picture coding comprising:
   means for receiving and storing picture data composed in frames,
   activity calculating means for calculating the activity of the picture data in every frame,
   frame/field coding judging means for receiving the activity, and judging to perform frame unit coding when the activity is over a specific value or to perform field unit coding by dividing a frame into fields when the activity is below a specific value, and
   coding means for coding in frame unit or coding in field unit concerning the picture data on the basis of the judgement, and issuing a coded picture signal containing the frame/field coding judgement signal.

6. A method for picture decoding comprising:
   a step of receiving a coded picture signal and extracting a frame/field coding judging signal from the coded picture signal input,
   a step of issuing a signal for changing over decoding action in frame unit or field unit depending on the frame/field coding judging signal, and

a step of decoding the coded picture signal in frame unit or field unit according to the changeover signal.

7. An apparatus for picture decoding comprising:

means for receiving a coded picture signal and extracting a frame/field coding judging signal from the coded picture signal input,

frame/field decoding changeover means for issuing a signal for changing over decoding action in frame unit or field unit, and

decoding means for decoding the coded picture signal in frame unit or field unit according to the changeover signal.

Fig. 1

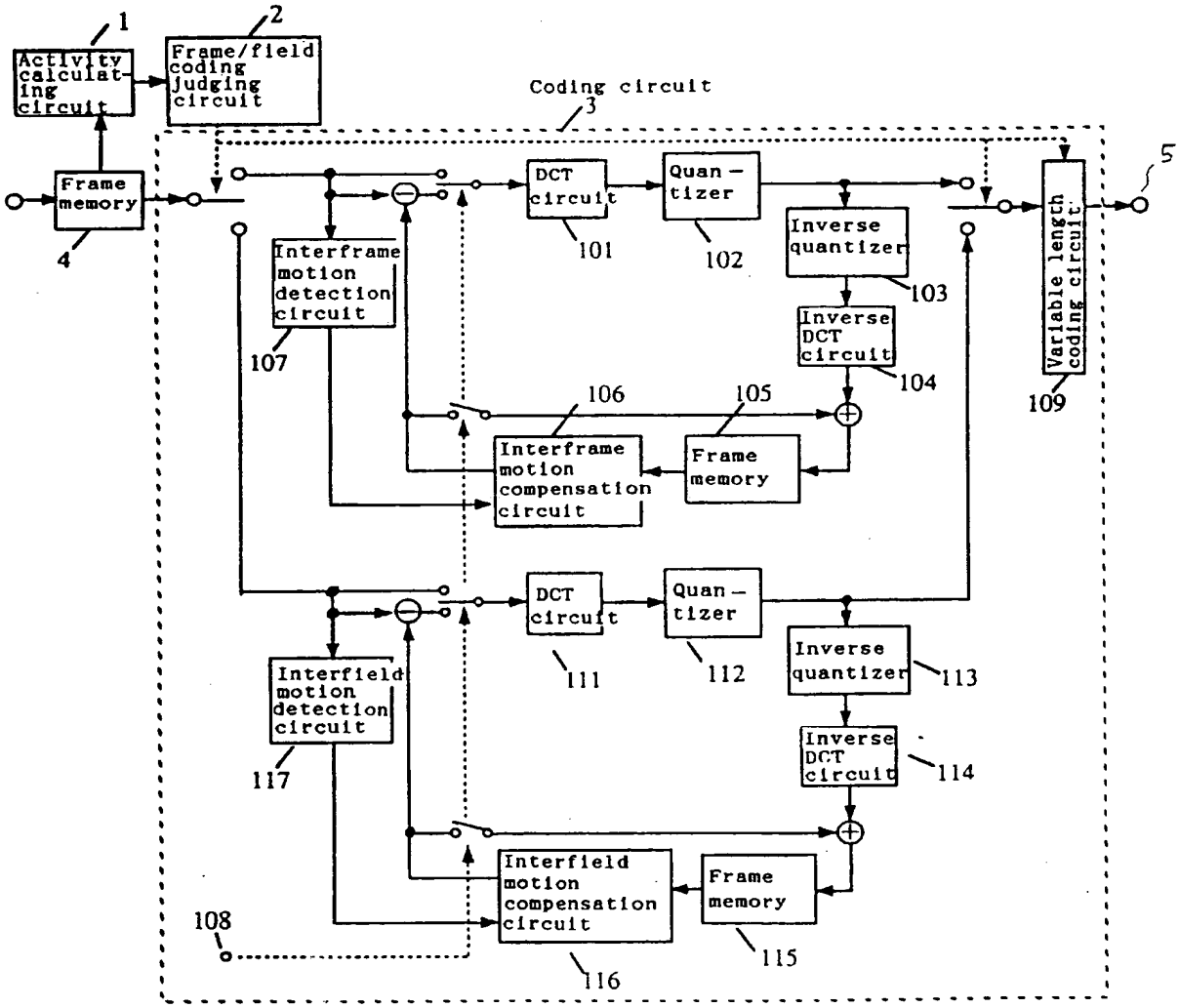

1
Activity calculating circuit
2
Frame/field coding judging circuit
Coding circuit
3
Frame memory
4
5
DCT circuit
101
Quantizer
102
Inverse quantizer
103
Inverse DCT circuit
104
Variable length coding circuit
109
Interframe motion detection circuit
107
106
105
Interframe motion compensation circuit
Frame memory
DCT circuit
111
Quantizer
112
Inverse quantizer
113
Inverse DCT circuit
114
Interfield motion detection circuit
117
Interfield motion compensation circuit
116
Frame memory
115
108

Fig. 2

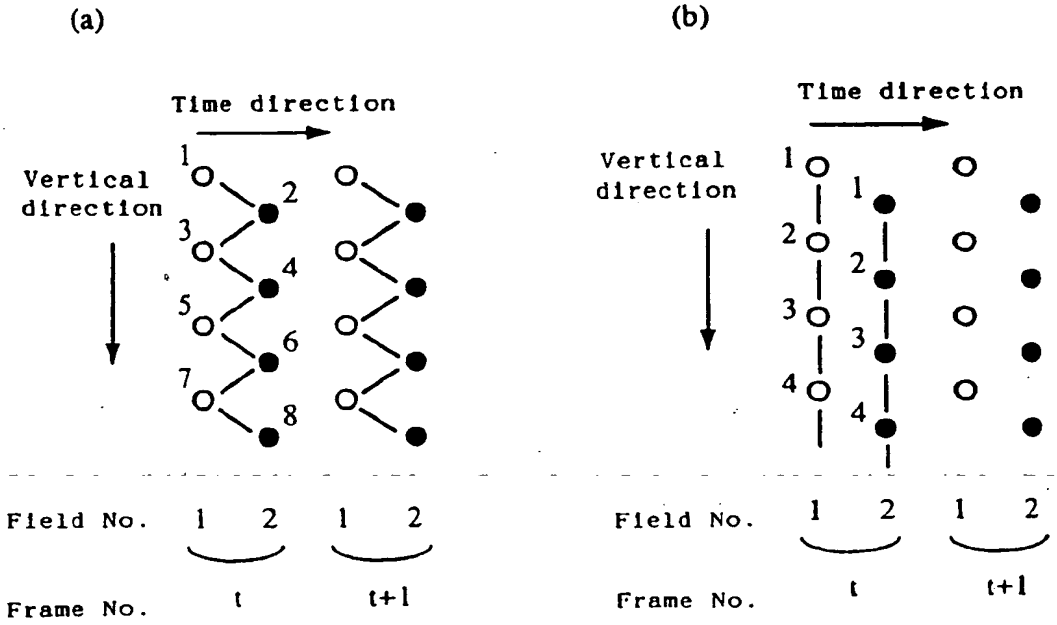

(a)
Time direction
Vertical direction
1
2
3
4
5
6
7
8
Field No. 1 2 1 2
Frame No. t t+1
(b)
Time direction
Vertical direction
1
2
3
4
1
2
3
4
Field No. 1 2 1 2
Frame No. t t+1

Fig. 3

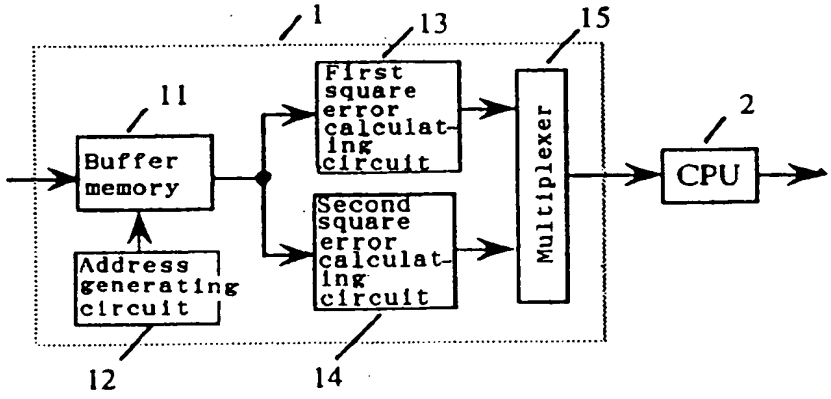

1
13
15
11
First square error calculating circuit
Buffer memory
Multiplexer
2
CPU
Second square error calculating circuit
Address generating circuit
12
14

Fig. 4

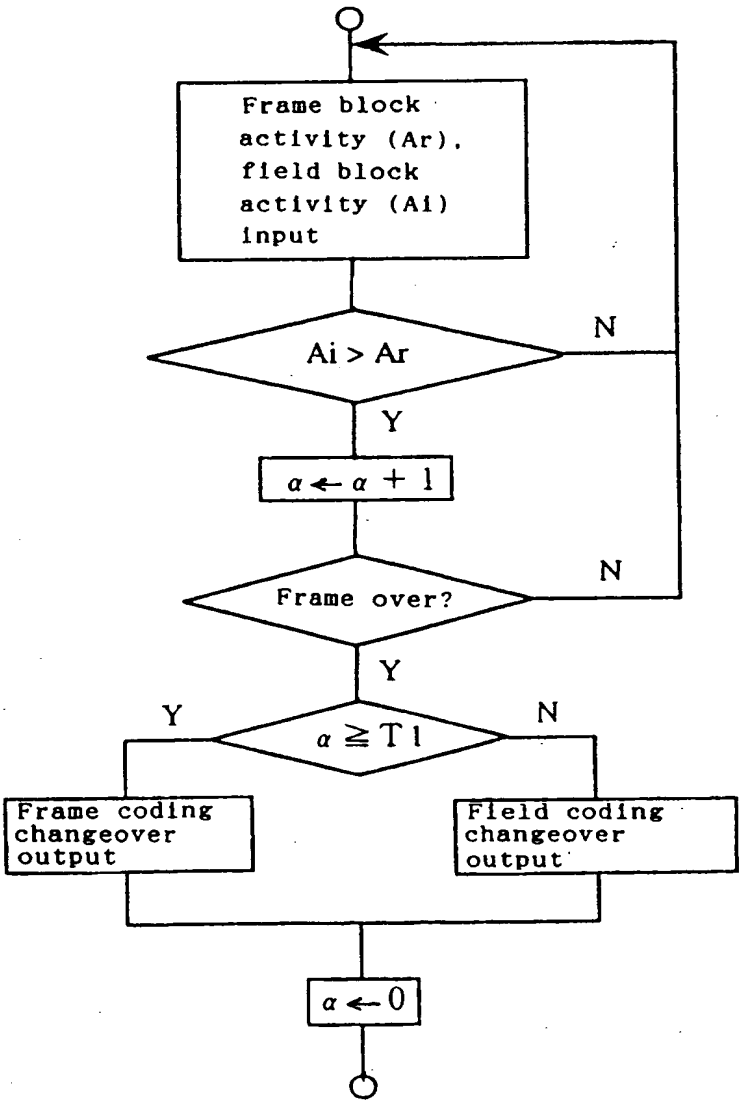

Frame block activity (Ar), field block activity (Ai) input
Ai > Ar
N
Y
α ← α + 1
Frame over?
N
Y
Y
α ≧ T1
N
Frame coding changeover output
Field coding changeover output
α ← 0

Fig. 5

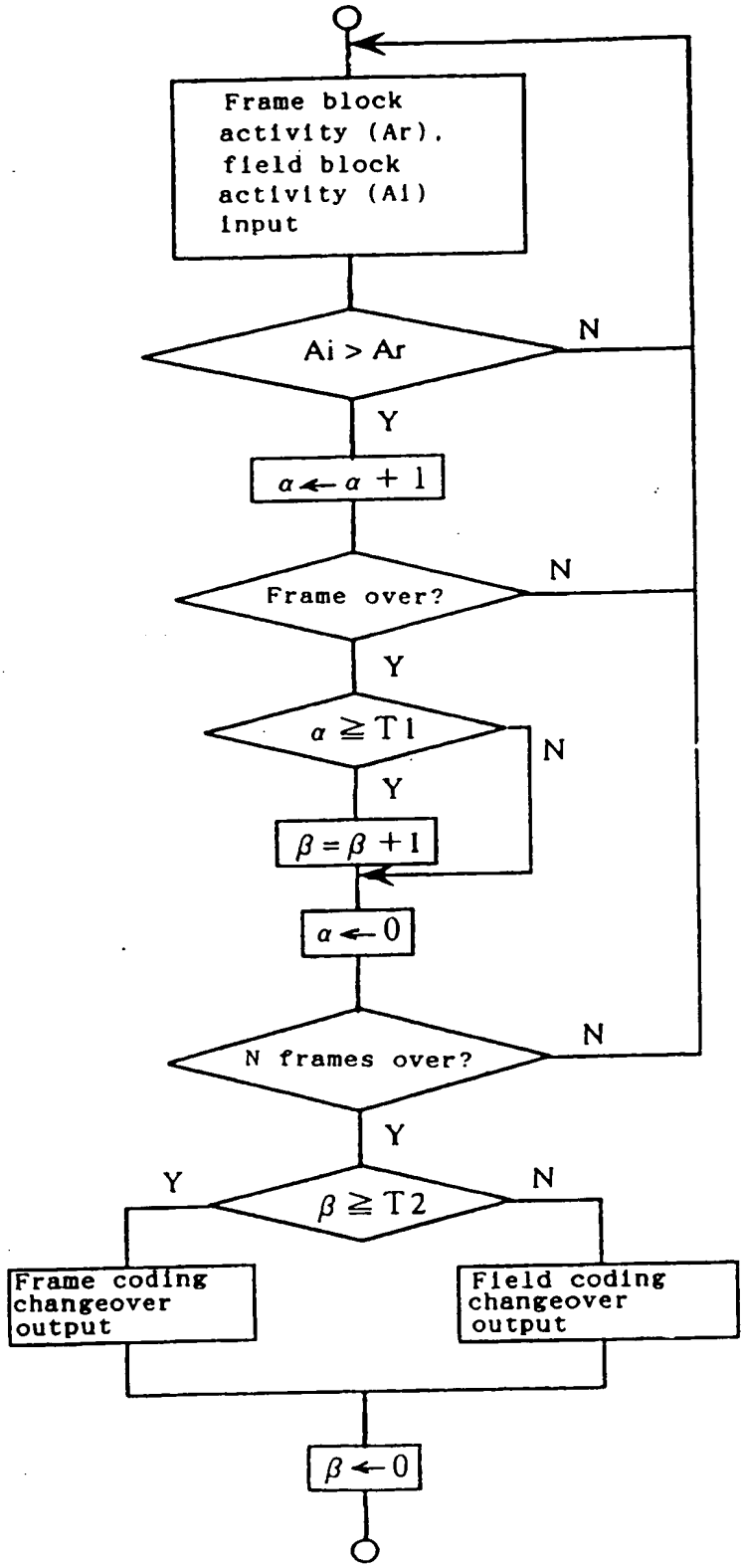

Frame block activity (Ar), field block activity (Ai) input
Ai > Ar
N
Y
α ← α + 1
Frame over?
N
Y
α ≧ T1
N
Y
β = β + 1
α ← 0
N frames over?
N
Y
Y
β ≧ T2
N
Frame coding changeover output
Field coding changeover output
β ← 0

Fig. 6

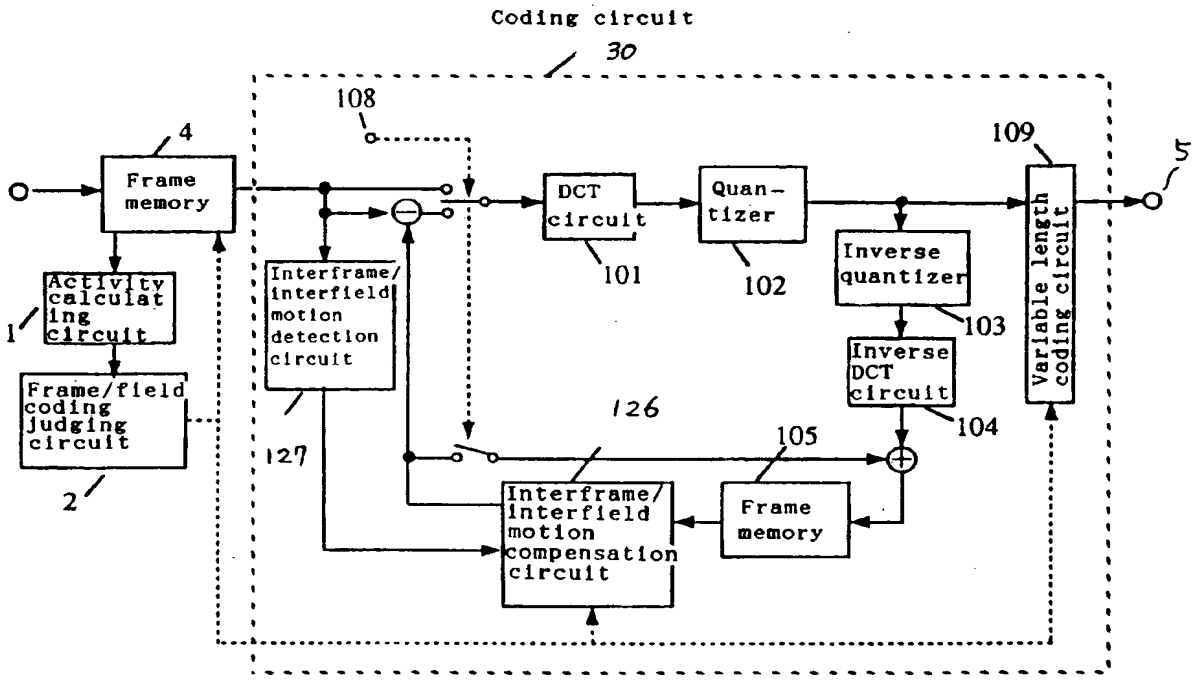

Coding circuit
30
108
4
Frame memory
109
5
DCT circuit
Quan-tizer
Inverse quantizer
Variable length coding circuit
Activity calculating circuit
1
Interframe/ interfield motion detection circuit
101
102
103
Inverse DCT circuit
104
Frame/field coding judging circuit
2
126
127
105
Interframe/ interfield motion compensation circuit
Frame memory

Fig. 7

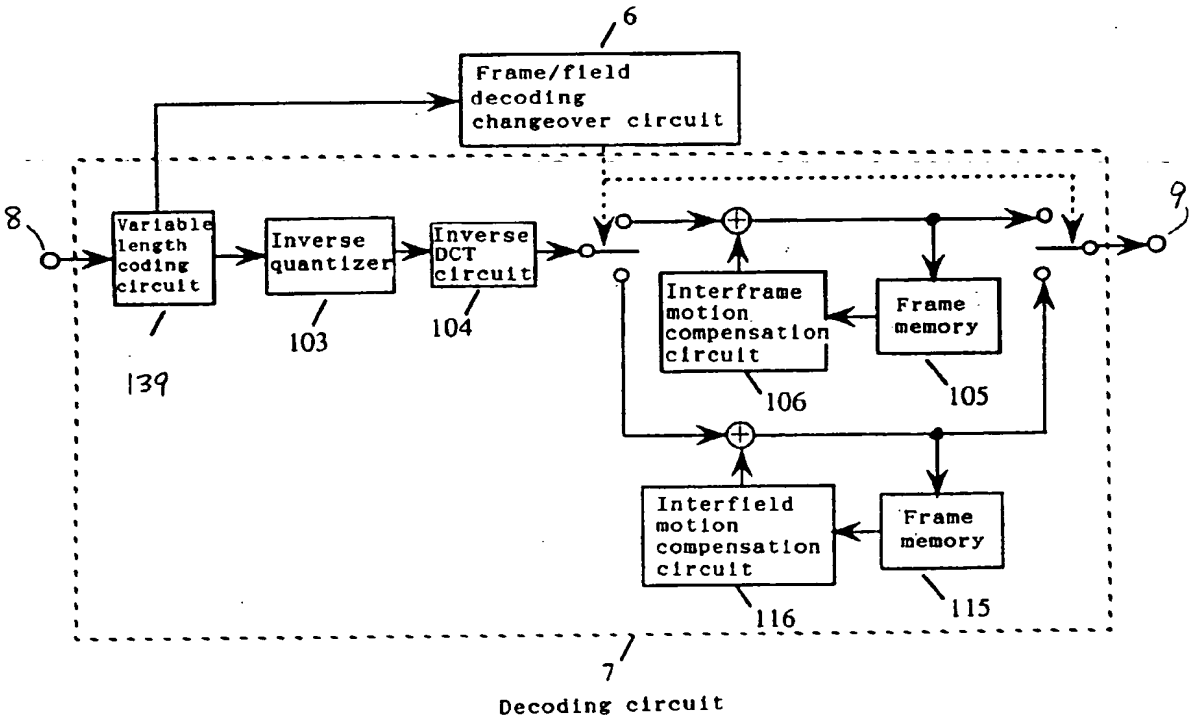
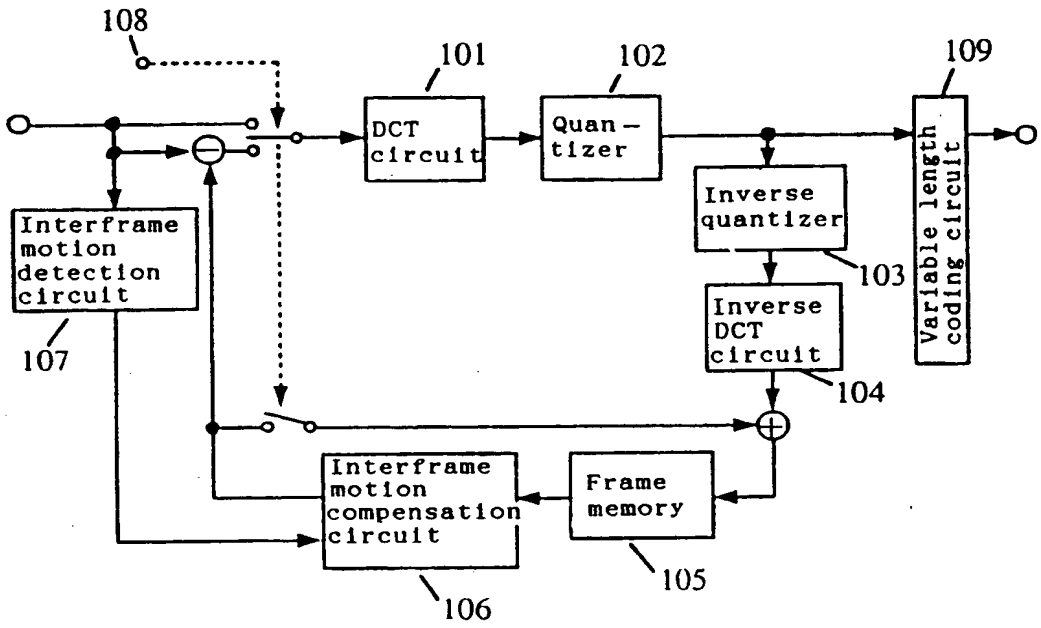
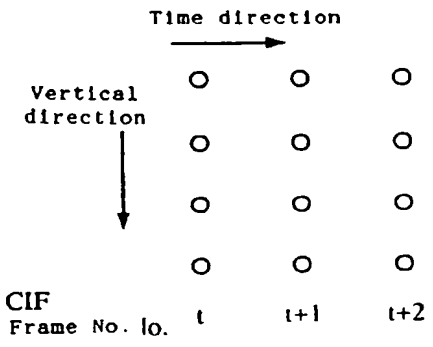

6
Frame/field decoding changeover circuit
8
Variable length coding circuit
139
Inverse quantizer
103
Inverse DCT circuit
104
9
Interframe motion compensation circuit
106
Frame memory
105
Interfield motion compensation circuit
116
Frame memory
115
7
Decoding circuit

Fig. 8



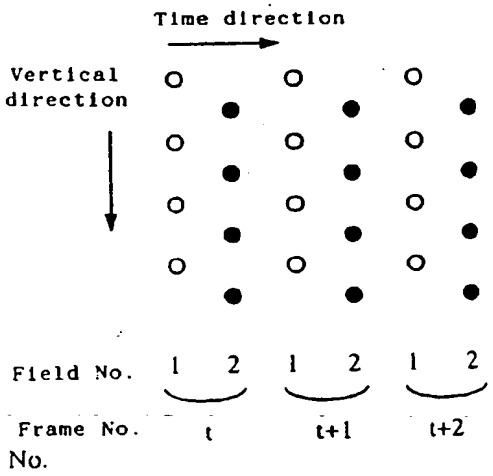
PRIOR ART

Fig. 9



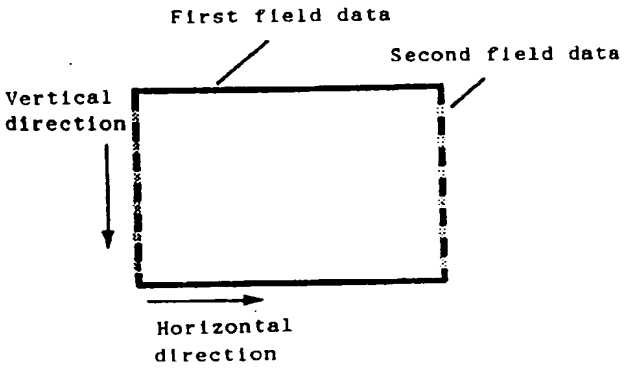
PRIOR ART

Fig. 10



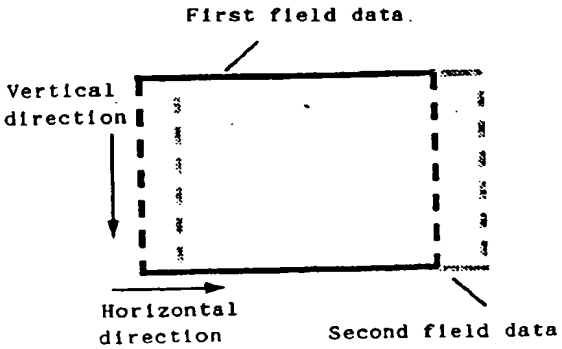
PRIOR ART

Fig. 11



PRIOR ART

Fig. 12



PRIOR ART

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 599 529 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93309121.7**

(22) Date of filing : **15.11.93**

(51) Int. Cl.[5] : **H04N 7/13**, H04N 7/137, H04N 7/26, H04N 7/30, H04N 7/50, H04N 7/36

(30) Priority : **25.11.92 JP 314815/92**

(43) Date of publication of application : **01.06.94 Bulletin 94/22**

(84) Designated Contracting States : **DE FR GB IT NL**

(88) Date of deferred publication of search report : **06.09.95 Bulletin 95/36**

(71) Applicant : **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
1006, Oaza Kadoma
Kadoma-shi, Osaka-fu, 571 (JP)

(72) Inventor : **Takahashi, Toshiya**
1-5-107, Akeno-cho
Takatsuki-shi, Osaka, 569 (JP)

(74) Representative : **Crawford, Andrew Birkby et al**
A.A. THORNTON & CO.
Northumberland House
303-306 High Holborn
London WC1V 7LE (GB)

(54) Method and apparatus for picture coding and method and apparatus for picture decoding.

(57) Method and apparatus for picture coding and method and apparatus for picture decoding are disclosed, wherein an apparatus for picture coding comprises :

means for receiving and storing picture data composed in frames,

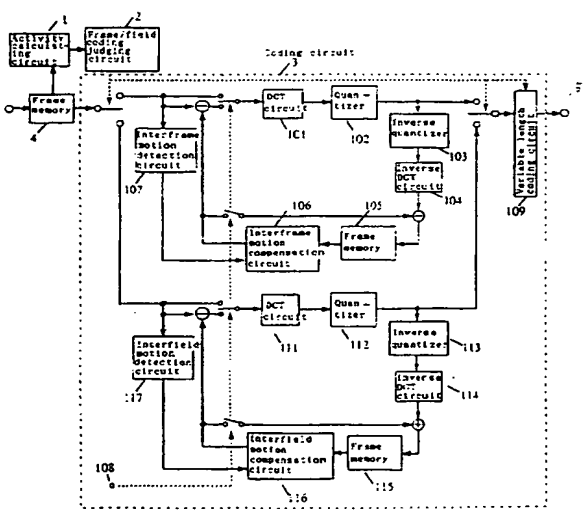
activity calculating means for calculating the activity of the picture data in every frame,

frame/field coding judging means for receiving the activity, and Judging to perform frame unit coding when the activity is over a specific value or to perform field unit coding by dividing a frame into fields when the activity is below a specific value, and

coding means for coding in frame unit or coding in field unit concerning the picture data on the basis of the judgement, and issuing a coded picture signal containing the frame/field coding Judgement signal,

whereby picture coding of high efficiency is realized despite magnitude of motion, by coding in field unit when the motion of picture is large, and coding in frame unit by making use of the vertical correlation of picture when the motion is small.

Fig. 1



EP 0 599 529 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 9121

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X Y	US-A-4 217 609 (HATORI ET AL.) * column 10, line 21 - line 35 *	1,5-7 2-4	H04N7/13 H04N7/137 H04N7/26 H04N7/30 H04N7/50 H04N7/36
Y	SIGNAL PROCESSING IMAGE COMMUNICATION., vol. 4, no. 4/5, August 1992 AMSTERDAM NL, pages 379-387, OHTSUKA ET AL. 'Development of 135 Mbit/s HDTV codec' * page 380, column 2, line 1 - line 25; figure 1 *	1	
Y	WO-A-87 04033 (BRITISH BROADCASTING CORPORATION) * page 2, line 13 - page 4, line 3 *	1-4	
A	PATENT ABSTRACTS OF JAPAN vol. 7 no. 251 (E-209) ,8 November 1983 & JP-A-58 137379 (NIPPON DENKI K.K.) 15 August 1983, * abstract *	1-7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
A	US-A-3 761 613 (LIMB) * column 3, line 44 - column 11, line 20 *	1-7	H04N
A	SIGNAL PROCESSING IMAGE COMMUNICATION., vol. 2, no. 3, October 1990 AMSTERDAM NL, pages 333-341, IRIE ET AL. 'ADAPTIVE SUB-BAND DCT CODING FOR HDTV SIGNAL TRANSMISSION' * page 334, column 1, line 16 - page 336, column 2 *	1-7	
A	EP-A-0 510 972 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) * column 3, line 36 - column 4, line 48 *	1-7	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	30 June 1995	Materne, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)